

CLAIMS

What is claimed is:

1. A power supply over-drive protection system for a DUT comprising:

5        a processor coupled to a memory via a bus, said memory having  
instructions that when executed implement a method of monitoring power  
coupled to said DUT comprising:

a) determining whether an activity signal from a DUT is received, said  
activity signal generated by said DUT when said DUT is coupled to an

10      external power source;

b) if said activity signal is received in a), generating a signal for  
preventing the coupling of power to said DUT from an in circuit emulator;

c) if said activity signal is not received in a), coupling power to said  
DUT from said in circuit emulator;

15        d) if said activity signal is not received in response to c), decoupling  
power to said DUT from said in circuit emulator and generating a fault  
condition signal.

20        2. A system as described in Claim 1 wherein said DUT is a  
microcontroller.

25        3. A system as described in Claim 1 wherein said DUT is located on a  
pod configured to couple said DUT to a power source in said in circuit  
emulator.

4. A system as described in Claim 1 wherein said step a) and said  
step d) are configured to prevent a simultaneous coupling of said DUT to  
more than one power source.
- 5           5. A system as described in Claim 1 wherein said activity signal from  
said DUT is a clock signal.

6. A system as described in Claim 1 wherein said DUT is located on a  
pod coupled to said in circuit emulator using a cable.

- 10           10. 7. A system as described in Claim 1 wherein said fault condition signal  
comprises setting a memory location bit to indicate a fault occurrence.
- 15           15. 8. A method for protecting a DUT from a power supply over-drive  
condition comprising:  
a) determining whether an activity signal from a DUT is received, said  
activity signal generated by said DUT when said DUT is coupled to an  
external power source;
- 20           20. b) if said activity signal is received in a), generating a signal for  
preventing the coupling of power to said DUT from an in circuit emulator;  
c) if said activity signal is not received in a), coupling power to said  
DUT from said in circuit emulator;

d) determining whether said activity signal is received in response to  
c); and

e) if said activity signal is not received in d), decoupling power to said  
DUT from said in circuit emulator and generating a fault condition signal.

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9. A method as described in Claim 8 wherein said DUT is a  
microcontroller .

10. A method as described in Claim 8 wherein said DUT is located on  
a pod configured to couple said DUT to a power source in said in circuit  
emulator.

11. A method as described in Claim 8 wherein said step a) and said  
step d) are configured to prevent a simultaneous coupling of said DUT to  
15 more than one power source.

12. A method as described in Claim 8 wherein said activity signal from  
said DUT is a clock signal.

20 13. A method as described in Claim 8 wherein said DUT is located on  
a pod coupled to said in circuit emulator using a cable.

14. A method as described in Claim 8 wherein said fault condition signal comprises setting a memory location bit to indicate a fault occurrence.

15. An external power detection and power supply over-drive

5 protection system for a DUT comprising:

a host computer system;

an in circuit emulator coupled to said host computer system, said in circuit emulator having an in circuit emulator power source for activating a DUT;

10 a pod coupled to said in circuit emulator and coupled to said DUT; and an external power source for activating said DUT;

wherein said host computer system includes a memory having computer readable instructions that when executed by the host computer system implement a method of supervising the coupling of power to said DUT

15 comprising:

a) detecting whether an activity signal is generated by said DUT, said activity signal caused by coupling said DUT to said external power source

b) if said activity signal is detected in a), generating a signal for preventing the coupling said DUT to said in circuit emulator power source;

20 c) if said activity signal is not detected in a), coupling said in circuit emulator power source to said DUT; and

d) in response to c), if said activity signal is not detected, decoupling power to said DUT from said in circuit emulator power source and generating a fault signal.

5        16. A system according to Claim 15 wherein said DUT is a microcontroller.

17. A system according to Claim 15 wherein said in circuit emulator comprises a field programmable gate array capable of emulating said DUT.

10      18. A system according to Claim 15 wherein said activity signal from said DUT is a clock signal.

15      19. A system according to Claim 15 wherein said DUT is located on a pod coupled to said in circuit emulator by a CAT5 cable.

20      20. A system according to Claim 15 wherein said fault signal comprises a bit set in a memory location recognizable as said fault signal.

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